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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Claims 1-9, 11, 12 and 14-28 are pending.

Claims 10 and 13 are cancelled.

Claims 1-9, 11, 12 and 14-28 are rejected.

Claim Rejections - 35 USC § 102

1.　　The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.　　Claims 1-5, 7-8, 11-12, 15-171 19-20, and 23-26 are rejected under 35

U.S.C. 102(e) as being anticipated by Wybenga et al. (US2004/0223504, hereinafter

Wybenga).

　　　Regarding claims 1, Wybenga et al. disclose Apparatus and method for

workflow-based routing in a distributed architecture router (see paragraph 9 line 1-4)

comprising: at least one node interconnected through a fabric (paragraphs 0035, routing

nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-

speed switch fabrics 155a and 155b), the at least one node (see paragraph 35 line 6

routing nodes) comprising a plurality of network processing devices (see figure 2 box

230 classification processor box 240 system processor box 250 async variables

controller, Network Processor 260), at least one network processing device for receiving at least one of the cell and the packet information, for determining a destination within the node for the cell and the packet information, and for at least one of routing and forwarding the cell and the packet information to the destination (see paragraph 21 line 5-15); a shared bus structure for coupling each of the network processing devices with each other (see paragraph 40 line 3 PCI bus and figure 2 ref 290, where figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260 are coupled to each other using bus 290. Network Processor 260 is coupled to rest of the mentioned processor using bus 290 via PCI Bridge 270); and an interface (see figure 2 box 280 GBE which interfaces figure 1 box 150 switch fabric) for coupling the at least one processing devices with the fabric (see figure 2 box 280 GBE interconnects with box 260 network processor wherein 280 GBE which interfaces figure 1 box 150 switch fabric) to support communication between nodes via (paragraphs 0035, routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b) a coupling means (figure 2, 280 GBE) different from the shared bus structure (figure 2, 280 GBE, being different from bus 290).

Regarding claims 27, Wybenga discloses a digital communication system (system in figure 1) for processing at least one of cell and packet information (see abstract), comprising: at least one node interconnected through a fabric (paragraphs 0035, routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b), the at least one node (see

paragraph 35 line 6 routing nodes) comprising: a plurality of network processing devices
(see figure 2 box 230 classification processor box 240 system processor box 250 async
variables controller, Network Processor 260), at least one network processing device
being operable to receive the at least one of cell and packet information, to determine a
destination within the node for the at least one of cell and packet information, and to
provide at least one of routing and forwarding of the at least one of cell and packet
information to the destination (see paragraph 21 line 5-15); a shared bus structure
coupled to each network processing device to support communications between
network processing devices (see paragraph 40 line 3 PCI bus and figure 2 ref 290,
where figure 2 box 230 classification processor box 240 system processor box 250
async variables controller, Network Processor 260 are coupled to each other using bus
290. Network Processor 260 is coupled to rest of the mentioned processor using bus
290 via PCI Bridge 270); and an interface (see figure 2 box 280 GBE which interfaces
figure 1 box 150 switch fabric) for coupling the at least one network processing device
with the fabric (see figure 2 box 280 GBE interconnects with box 260 network processor
wherein 280 GBE which interfaces figure 1 box 150 switch fabric) to support
communication between nodes (paragraphs 0035, routing nodes 110, 120, 130 and
140, connected by switch 150, which comprises a pair of high-speed switch fabrics
155a and 155b) via a coupling means (figure 2, 280 GBE) different from the shared bus
structure (figure 2, 280 GBE, being different from bus 290).

Regarding claim 2, Wybenga et al. teaches the destination is determined in response to at least one of stored routing rules and characteristics of the cell and the packet information (see paragraph 39 line 14 classification processor).

Regarding claim 3, Wybenga et al. teaches the at least one of a plurality of network processing devices employ dynamically updated routing rules (see paragraph 36 line 5-8).

Regarding claim 4, Wybenga et al. teaches the at least one of a plurality of network processing devices performs the at least one of routing and forwarding on both the cell and the packet information simultaneously (see paragraph 46).

Regarding claim 5, Wybenga et al. teaches the at least one of a plurality of network processing devices directly delivers the at least one of routing and forwarding the cell and the packet information into a memory of the destination (see paragraph 36 line 5-10).

Regarding claim 7, Wybenga et al. teaches the interface provides the cell and the packet information to the at least one network processing device (see paragraph 36 line 6-7).

Regarding claim 8, Wybenga et al. teaches the interface comprises at least one of a System Interface (see figure 142 PMD module) and a it Maintenance Interface (see paragraph 41 line 8 doorbell register interface).

Regarding claim 11, Wybenga et al. teaches the node further comprises: a general-purpose processor (see paragraph 41 line 6-16 and figure 2 box 240 system

processor) for at least one of controlling the plurality of network processing devices and performing maintenance on the node (see paragraph 42).

Regarding claim 12, Wybenga et al. teaches the shared bus structure couples the general-purpose processor with each of the network processing devices (see figure 2 ref 290).

Regarding claim 15, Wybenga et al. teaches comprising: at least one external system input/output interface (see figure 1 box 146 IOP).

Regarding claim 16, Wybenga et al. teaches the external system input/output interface supports at least one transport mechanism type, the at least one transport mechanism type comprising at least one of Asynchronous Transfer Mode, Internet Protocol, and Frame Relay (see paragraph 36 line 13- 14).

Regarding claim 17, Wybenga et al. teaches a communication node for processing at least one of cell and packet information comprising: a plurality of network processing devices (see figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260) at least one network processing device for receiving at least one of the cell and the packet information(see figure 2 box 230 classification processor box 240 system processor box 250 async variables controller), for determining a destination within the node for the cell and the packet information, and for at least one of routing and forwarding the cell and the packet information to the destination (see paragraph 21 line 5-15), the destination determined in response to at least one of stored routing rules and characteristics of the cell and the packet information (see paragraph 39 line 14 classification processor); a

shared bus structure for coupling each of the network processing devices with each other (see paragraph 40 line 3 PCI bus and figure 2 ref 290, where figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260 are coupled to each other using bus 290. Network Processor 260 is coupled to rest of the mentioned processor using bus 290 via PCI Bridge 270); and at least one of a System Interface (see figure 2 box 280 Gbe which interfaces with figure 1 box 150 switch fabric) and a Maintenance Interface (see paragraph 41 doorbell register interface where a doorbell interrupt is initiated when a device performs a write operation to a pre-defined Configuration Data Register. This interrupt can be enabled and disabled. Thus provide maintenance through an interface) coupled to at least one network processing device (see figure 2 box 280 GBE interconnects with box 260 network processor wherein 280 GBE which interfaces figure 1 box 150 switch fabric) via a coupling means (figure 2, 280 GBE and two sided arrow connecting PCI bridge 270 to network processor 260) different from the shared bus structure (figure 2, 280 GBE and two sided arrow connecting PCI bridge 270 to network processor 260, being different from bus 290).

Regarding claims 19-20 and 23-26, Wybenga et al. disclose all the limitations as discussed in the rejection of claims 3-5, and 11-13, and 15 and are therefore claims 18-21 and 23-26 are rejected using the same rationales.

In regards to claim 28, Wybenga teaches the interface comprising: at least one of a System Interface (see figure 2 box 280 Gbe which interfaces with figure 1 box 150 switch fabric) and a Maintenance Interface.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

3.   Claims 3 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wybenga et al. in view of Sundling et al. (US6785277).

Regarding claims 3 and 18, Wybenga et al. disclose all the subject matter of the

claimed invention with the exception of the at least one of a plurality of network

processing devices employ dynamically updated routing rules. Sundling et al. from the

same or similar fields of endeavor teaches the use of cost factors change, all or some of

the respective routing tables must be modified to properly utilize this information (see

Sundling et al. column 9 line 65 to column 10 line 10). Thus, it would have been obvious

to one of ordinary skill in the art at the time of the invention to use the cost factors

change as taught by Sundling et al. in apparatus and method for workflow-based routing

in a distributed architecture router of Wybenga et al. in order to provide update

routing transmission services.

4.   Claims 6, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Wybenga et al. in view of its background.

        Regarding claims 6, 14 and 21, Wybenga et al. disclose all the subject matter of

the claimed invention with the exception of the at least one network processing device

supports peer-to-peer routing. Wybenga et al. background from the same or similar

fields of endeavor teaches the use of new services, such as voice-over-IP (VoIP) or

streaming applications, and the development of mobile Internet (see Wybenga et al.

background paragraph 2) which are forms of peer-to-peer system. Thus, it would have

been obvious to one of ordinary skill in the art at the time of the invention to use the new

services, such as voice-over-IP (VoIP) or streaming applications, and the development

of mobile Internet as taught by the background of Wybenga et al. in apparatus and

method for workflow-based routing in a distributed architecture router of Wybenga et al.

in order to provide peer-to-peer system service and system transmission method.

5.   Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wybenga et al. in view of Oner (US2005/0078696).

Regarding claims 9 and 22, Wybenga et al. teaches the interface comprises at least one of a System Interface (see figure 142 PMD module) and a Maintenance Interface (see paragraph 41 line 8 doorbell register interface), and disclose all the subject matter of the claimed invention with the exception of the interface comprises a multiplexer for creating a multiplexed stream from the at least one of the cell and the packet information. Oner from the same or similar fields of endeavor teaches the use of address multiplexer (see Oner paragraph 125 line 9 and figure 9 box 92 address multiplexer). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the address multiplexer as taught by Oner in apparatus and method for workflow-based routing in a distributed architecture router of Wybenga et al. in order to enhance the efficiency of the system.

Response to Arguments

6.   Applicant's arguments see pages 7-10 of the Remarks section, filed 8/19/2008, with respect to the rejections of the claims have been fully considered and are not persuasive.

Applicant argues (page 8 first paragraph) that the interface device (see Fi.q. 2, 280) does not couple any of the network processing devices (see Fiq. 2, 230,240, 250) to the fabric (see Fi.q. 1,150) throu.qh any coupling means different from the shared bus structure (see Fiq. 2, 290) as recited in amended claim 1. However, Examiner respectfully disagrees with the Applicant's assertion. The cited prior art does indeed teach the cited limitations. Specifically, cited prior art teaches an interface (see

figure 2 box 280 GBE which interfaces figure 1 box 150 switch fabric) for coupling the at

least one processing devices with the fabric (see figure 2 box 280 GBE interconnects

with box 260 network processor wherein 280 GBE which interfaces figure 1 box 150

switch fabric) to support communication between nodes via (paragraphs 0035, routing

nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-

speed switch fabrics 155a and 155b) a coupling means (figure 2, 280 GBE) different

from the shared bus structure (figure 2, 280 GBE, being different from bus 290).

Applicant argues (page 8 last paragraph) that the System Interface (see Fig. 2,

280) is not coupled to any of the network processinq devices (see Fig. 2, 230, 240, 250)

via a coupling means different from the shared bus structure (see Fig. 2, 290) as recited

in amended claim 17. However, Examiner respectfully disagrees with the Applicant's

assertion. The cited prior art does indeed teach the cited limitations. Specifically, cited

prior art teaches one of a System Interface (see figure 2 box 280 Gbe which interfaces

with figure 1 box 150 switch fabric) and a Maintenance Interface (see paragraph 41

doorbell register interface where a doorbell interrupt is initiated when a device

performs a write operation to a pre-defined Configuration Data Register. This interrupt

can be enabled and disabled. Thus provide maintenance through an interface) coupled

to at least one network processing device (see figure 2 box 280 GBE interconnects with

box 260 network processor wherein 280 GBE which interfaces figure 1 box 150 switch

fabric) via a coupling means (figure 2, 280 GBE and two sided arrow connecting PCI

bridge 270 to network processor 260) different from the shared bus structure (figure 2,

280 GBE and two sided arrow connecting PCI bridge 270 to network processor 260,

being different from bus 290).

Claims 3, 6, 9, 14, 18, 21 and 22 are not allowable for the same reasons cited

above.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to SALMAN AHMED whose telephone number is

(571)272-8307. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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/Salman Ahmed/

Examiner, Art Unit 2419